A SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority from Japanese patent application JP 2003-084738 filed on March 26, 2003, the content of which is hereby incorporated by reference into this application.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and particularly to a technique which is effectively applicable to the reduction in size of a module such as a power amplifier module.

As a structure involving a reduced size of a semiconductor device there is known an SCP (Stacked Chips Package) structure in which semiconductor chips are arranged in a superimposed fashion. In the SCP, a lower-layer chip is provided and an upper-layer chip smaller than the lower-layer chip is superimposed on the lower-layer chip, and thus chips are stacked in two stages to attain the reduction of size (see, for example, Patent Literature 1).

Patent Literature 1:

Japanese Patent Publication Laid-Open

No. Hei 7(1995)-58280 (page 3, Fig. 2)

SUMMARY OF THE INVENTION

Many electronic parts are incorporated in a communication terminal such as a portable telephone, and a high frequency amplifier (power amplifier module) incorporated in a transmission system of the portable telephone is rapidly becoming smaller in size and higher in function. As one of communication methods there is known a GSM (Global System for Mobile Communications) method.

At present, an external size of a power amplifier module for the GSM method is 10 mm long by 8 mm wide, but as to the next-generation module it is presumed that a size of 6 mm long by 5 mm wide will become popular.

Also in the field of CDMA (Code Division Multiple Access) it can be presumed that there will occur demands for successively smaller sizes from the present size of 6 mm long by 6 mm wide to the size of 5 mm long by 5 mm wide and further to the size of 4 mm long by 4 mm wide.

In such an ultra-small-sized power amplifier module, by only a two-dimensional parts' packaging on a surface of a module substrate of a wiring substrate configuration, semiconductor chips with active elements such as transistors incorporated therein, as well as passive elements as chip parts such as resistors (chip resistors) and capacitors (chip capacitors), can no longer be mounted, and a three-dimensional packaging becomes necessary.

For attaining the reduction in size of a power amplifier module, the present inventors have made studies about a stacked structure of semiconductor chips and, as a result, found out the following problems.

If a stacked structure semiconductor chips is adopted in a power amplifier module, then as to an upper chip disposed on a lower chip, its GND (ground) connection is difficult to be done on the back side of the chip and therefore it is difficult to ensure a large area of GND with respect to the upper chip. Thus, for example, in the case where a power amplifier module has amplifier circuits which amplify an input signal in three stages, it is only the first-stage of an amplifier circuit that can be incorporated in an upper-stage chip.

As a result, the second- and third-stage amplifier circuits are incorporated in a lower chip, resulting in that the difference in size between the upper- and lower-stage chips becomes large and both are unbalanced in size, thus giving rise to the problem that it is impossible to attain a satisfactory reduction in size of the module product.

Further, since the size of the upper-stage chip is small, the wire length becomes large, that is, it becomes difficult to carry out an assembling process.

It is an object of the present invention to provide a semiconductor device capable of attaining the reduction in size.

It is another object of the present invention to provide a

semiconductor device capable of improving the reliability thereof.

It is a further object of the present invention to provide a semiconductor device capable of improving the assemblability thereof.

The above and other objects and novel features of the present invention will become apparent from the following description and the accompanying drawings.

The following is a brief description of a typical mode of the invention as disclosed herein.

According to the present invention there is provided a semiconductor device comprising a first semiconductor chip with elements formed on a semiconductor substrate; a second semiconductor chip with elements formed on a semiconductor substrate; a wiring substrate having a main surface and a back surface, the second semiconductor chip mounted on the main surface of the wiring substrate, the first semiconductor chip stacked on the second semiconductor chip; and an electrode of a fixed potential disposed on the first semiconductor chip on the side opposed to the second semiconductor chip, the electrode of the fixed potential being electrically connected to the semiconductor substrate of the first semiconductor chip and to the wiring substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing the structure of a power amplifier module as an example of a semiconductor device according to a first embodiment of the present invention;

Fig. 2 is a back view thereof;

Fig. 3 is a planar layout diagram showing a layout example of parts mounted on a main surface of a wiring substrate in the power amplifier module;

Fig. 4 is a circuit block diagram showing a structural example of a high frequency amplifier circuit incorporated in the power amplifier module;

Fig. 5 is an enlarged partial sectional view showing in a partially cut-away state the structure of a bonded portion between a first semiconductor chip and a second semiconductor chip in the power amplifier module;

Fig. 6 is a sectional view showing the structure of a power amplifier module according to a modification of the first embodiment;

Fig. 7 is a sectional view showing the structure of a power amplifier module according to another modification of the first embodiment;

Fig. 8 is a sectional view showing the structure of a power amplifier module as an example of a semiconductor device according to a second embodiment of the present invention;

Fig. 9 is a back view thereof; and

Fig. 10 is a planar layout diagram showing a layout example

of parts mounted on a main surface of a wiring substrate in the power amplifier module of Fig. 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail hereinunder with reference to the accompanying drawings.

When required for convenience' sake, the following embodiments will be described in a divided manner into plural sections or embodiments, but unless otherwise mentioned, they are not unrelated to each other, but are in a relation such that one is a modification, a description of details, or a supplementary explanation, of part or the whole of the other.

In the following embodiments, when reference is made to the number of elements (including the number, numeral value, quantity, and range), no reference is made to the number referred to, but numerals above and below the number referred to will do as well unless otherwise mentioned and except the case where it is basically evident that limitation is made to the number referred to.

It goes without saying that in the following embodiments their constituent elements (including constituent steps) are not always essential unless otherwise mentioned and except the case where they are considered essential basically obviously.

Likewise, it is to be understood that when reference is made to the shapes and positional relation of components in the

following embodiments, those substantially closely similar to or resembling such shapes, etc. are also included unless otherwise mentioned and except the case where a negative answer results basically obviously.

In all of the drawings for illustrating the embodiments, portions having the same functions are identified by like reference numerals, and repeated explanations thereof will be omitted.

(First Embodiment)

Fig. 1 is a sectional view showing the structure of a power amplifier module as an example of a semiconductor device according to a first embodiment of the present invention, Fig. 2 is a back view thereof, Fig. 3 is a planar layout diagram showing a layout example of parts mounted on a main surface of a wiring substrate in the power amplifier module of Fig. 1, Fig. 4 is a circuit block diagram showing a structural example of a high frequency amplifier circuit incorporated in the power amplifier module of Fig. 1, Fig. 5 is an enlarged partial sectional view showing in a partially cut-away state the structure of a bonded portion between a first semiconductor chip and a second semiconductor chip in the power amplifier module of Fig. 1, Fig. 6 is a sectional view showing the structure of a power amplifier module according to a modification of the first embodiment, and Fig. 7 is a sectional view showing the structure of a power amplifier module

according to another modification of the first embodiment.

The semiconductor device of the first embodiment shown in Figs. 1 and 2 is a high frequency module product called a power amplifier module 1, having a stacked chip structure in which a second semiconductor chip is mounted on a main surface 4b of a module substrate (wiring substrate) 4 and a first semiconductor chip is superimposed on the second semiconductor chip. The semiconductor device of the first embodiment is mainly incorporated in a small-sized portable electronic device such as a portable telephone.

For example, the power amplifier module 1 is a high frequency amplifier which amplifies high frequencies (e.g., about 900 MHz and about 1800 MHz) in a portable telephone in plural stages.

In appearance, the power amplifier module 1 of this first embodiment comprises a quadrangular module substrate 4, a sealing portion 6 formed superimposedly on the main surface 4b of the module substrate 4, and plural external terminals 4f and an external terminal 4g for GND which are formed on a back surface 4c of the module substrate 4.

In assembling the power amplifier module 1, electronic parts, including semiconductor chips, are mounted onto a multi-substrate comprising plural module substrates 4 arranged side by side, then a sealing resin layer is formed at a predetermined certain height on an upper surface of the multi-

substrate so as to cover the electronic parts, and thereafter the multi-substrate, including the sealing resin layer superimposed thereon, is cut off longitudinally and transversely to afford plural power amplifier modules 1 at a time. Consequently, there is obtained a structure wherein side faces of each module substrate 4 and side faces of the sealing portion 6 are aligned with each other and end portions of the sealing portion 6 are not positioned outside end portions of the module substrate 4.

The module substrate 4 is constituted by a printed wiring substrate and has, for example, such a structure as a lamination of plural dielectric layers (insulating films). Conductor layers of predetermined wiring patterns are formed on the main surface 4b and the back surface 4c and also in the interior, the conductor layers on the main surface 4b and the back surface 4c being electrically connected with each other through via holes 4h or the like extending in the thickness direction of the substrate. In this first embodiment, the said dielectric layers are formed as five layers though no limitation is made thereto.

A detailed configuration of the power amplifier module 1 of this first embodiment will now be described. The power amplifier module 1 comprises a module substrate 4 as a wiring substrate having a main surface 4b and a back surface 4c on the side opposite to the main surface, a lower chip 7 as a second

semiconductor chip having elements formed on a semiconductor substrate 13, the lower chip 7 being mounted on the main surface 4b of the module substrate 4, an upper chip 2 as a first semiconductor chip having elements formed on a semiconductor substrate 13, the upper chip 2 being superimposed on the lower chip 7, a common electrode 12 of a fixed potential disposed on a back surface 2b of the upper chip 2, a plurality of electrically conductive wires 5 for connecting the upper chip 2 and the module substrate 4 electrically with each other, a plurality of chip parts 3 as passive parts mounted around the lower chip 7 and upper chip 2 on the module substrate 4, as shown in Fig. 3, and a sealing portion 6 formed so as to cover the lower chip 7, upper chip 2, plural wires 5 and plural chip parts 3 on the main surface 4b side of the module substrate 4. The common electrode 12 of a fixed potential is electrically connected to both the semiconductor substrate 13 of the upper chip 2 and the module substrate 4.

The back surface 2b of the upper chip 2, as an opposite side to the main surface 2a to which the wires 5 are connected, is opposed to the lower chip 7. As shown in Fig. 1, the lower chip 7 is mounted by flip connection (also called flip chip connection) in a cavity 4a as a recess formed in the module substrate 4 and is electrically connected to the module substrate 4 through bump electrodes 14.

The lower chip 7 is thus disposed in the cavity 4a which is

depressed relative to the main surface 4b of the module substrate 4. More specifically, the lower chip 7 is mounted face down onto the module substrate 4 so that its main surface 7a becomes opposed to the module substrate 4. The lower chip 7 is electrically connected to the module substrate 4 through bump electrodes 14 such as gold bumps, for example.

The upper chip 2 is mounted on a back surface 7b of the lower chip 7 in a stacked state and in a face up state with its main surface 2a facing up. Since the main surface 2a of the upper chip 2 thus faces up, the upper chip 2 is electrically connected to terminals 4e of the module substrate 4 through wires 5 such as gold wires, as shown in Fig. 3.

Next, a description will be given below of a high frequency amplifier circuit block shown in Fig. 4 in the power amplifier module of this first embodiment.

In the high frequency amplifier circuit, two frequency bands are amplified divided in two amplifier circuits each having a three-stage configuration. The amplifier circuit in each stage is controlled by a control IC (Integrated Circuit) 2h which is a bias circuit incorporated in the upper chip 2. In the power amplifier module of this first embodiment, the first- and second-stage amplifier circuits, out of the above three-stage amplifier circuits, are built in the upper chip 2, while the last-stage (third-stage) amplifier circuit is built in the lower chip 7.

A description will now be given of the two frequency bands which the power amplifier module 1 possesses. One is based on GSM (Global System for Mobile Communication) method, which uses a frequency band of 880 to 915 MHz, while the other is based on DCS (Digital Communication System 1800), which uses a frequency band of 1710 to 1785 MHz. The power amplifier module 1 matches both systems.

In the power amplifier module 1, as shown in Fig. 4, the high frequency amplifier circuit is divided into two types of circuit blocks 2e and 7e enclosed with dotted lines, and the upper chip 2 is adopted for the circuit block 2e, while the lower chip 7 is adopted for the circuit block 7e.

More specifically, in the power amplifier module 1 of this first embodiment, first- and second-stage amplifier circuits, which are relatively low in power consumption, are incorporated as the circuit block 2e into the upper chip 2, while the last-stage (third-stage) amplifier circuit, which is high in power consumption, is incorporated as the circuit block 7e into the lower chip 7.

Correspondingly to the circuit blocks 2e and 7e, a GSM-side first-stage amplifier 2c, a GSM-side second-stage amplifier 2f, a DCS-side first-stage amplifier 2d, and a DCS-side second-stage amplifier 2g, are incorporated in the upper chip 2, while a GSM-side last-stage (third-stage) amplifier 7c and a DCS-side last-stage (third-stage) amplifier 7d are incorporated in the

lower chip 7.

Upon receipt of a control signal, Vcontrol, the control IC 2h incorporated in the upper chip 2 controls the power of each of the GSM-side first-, second- and last-stage amplifiers 2c, 2f, 7c and also controls the power of each of the DCS-side amplifiers. In the power amplifier module 1 of this first embodiment, MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are used as amplifier elements, and in this case, the upper chip 2 controls the bias applied to the gate of each MOSFET, thereby controlling the power of outputs Pout (GSM) and Pout (DCS).

In the power amplifier module 1, as shown in Fig. 5, a common electrode 12 of a fixed potential is provided on each of the back surfaces 2b and 7b of the upper and lower chips 2, 7. More specifically, a common electrode 12 of a large area is formed throughout each of the back surface 7b of the lower chip 7 whose back surface is opposed to the upper chip 2 and the back surface 2b of the upper chip 2 whose back surface is opposed to the lower chip 7. In this case, since the upper chip 2 is stacked face up onto the back surface 7b of the lower chip 7, the back surfaces of both chips confront each other, and in this state the common electrode 12 formed on the back surface 7b of the lower chip 7 and the common electrode 12 formed on the back surface 2b of the upper chip 2 are electrically connected with each other using an electrically conductive

paste such as Ag paste 8.

Thus, as a fixed potential electrode of a large area, a common electrode 12 can be disposed between the upper and lower chips 2, 7, and by allowing the common electrode 12 of a large area to serve as GND electrode, it is possible to let GND electrode of a large area be present between the upper and lower chips 2, 7.

As shown in Figs. 1 and 5, the lower chip 7 has a projecting portion 7f projecting from the upper chip 2 and the common electrode 12 is also located on the projecting portion 7f of the lower chip 7. The common electrode 12 on the projecting portion 7f and GND terminals 4d on the module substrate 4 shown in Fig. 3 are connected together for grounding through electrically conductive gold wires 5.

As shown in Fig. 5, gold wires 5 are connected onto the projecting portion 7f of the lower chip 7 and therefore it is preferable Au (gold) plating film 9 be formed as surface layer in the common electrode 12. For example, the common electrode 12 comprises Ti (titanium) plating film 11 as an undercoat layer, Ni (nickel) plating film 10 as an intermediate plating layer, and Au plating film 9 as a surface plating layer. Thus, the common electrode 12 has a three-layer plating film structure.

For grounding of the lower chip 7, a predetermined bump electrode 14 for GND is connected to an external terminal 4g

for GND on the back surface 4c through a via 4h for GND formed in the module substrate 4, and thus GND of the lower chip 7 is strengthened. That is, GND of the lower chip 7 and GND of the common electrode 12 on the upper chip 2 are not common to each other. However, in the case where the grounding through the predetermined bump electrode 14 is not sufficient for the grounding of the lower chip 7, there may be adopted a configuration which uses both GND through the predetermined bump electrode 14 on the main surface 7a side of the lower chip 7 and GND using the common electrode 12 on the back surface 7b side.

In the power amplifier module 1 of this first embodiment, by adopting the foregoing stacked chip structure, GND of the upper chip 2 is connected to the module substrate 4 through the common electrode 12 disposed on the back surface 2b of the upper chip 2 and further through wires 5 connected to the common electrode 12, and thus can be strengthened. Accordingly, the first- and second-stage amplifier circuits, i.e., the first- and second-stage amplifiers 2c, 2f on the GSM side and the first- and second-stage amplifiers 2d, 2g on the DCS side can be incorporated in the upper chip 2.

Consequently, it is only the last-stage (third-stage) amplifier 7c on the GSM side and the last-stage (third-stage) amplifier 7d on the DCS side that are incorporated as amplifier elements (amplifier circuits) into the lower chip 7. As a

result, it is possible to make the upper chip 2 larger in size than a conventional like chip and make the lower chip 7 smaller in size than a conventional like chip.

That is, the difference in size between both chips can be made smaller than in the prior art.

As to the projecting portion 7f of the lower chip 7 projecting from the upper chip 2, it suffices for the projecting portion 7f to have an area for connection thereto of wires 5. It is preferable that the difference in size between the upper chip 2 and the lower chip 7 be as small as possible and that the ratio in projected area between the main surfaces 7a and 2a be in the range from 0.9 to 1.1

If these preferred conditions are satisfied, in the power amplifier module 1 of this first embodiment, it is possible to make both upper and lower chips 2, 7 almost equal in size. As a result, it is possible to reduce the area and hence reduce the size of the power amplifier module 1.

Moreover, since the size of the upper chip 2 can be made larger than in the prior art, the length of wires 5 for the upper chip 2 can be made short and as a result it is possible to improve the assemblability of the power amplifier module 1.

Further, since the common electrode 12 as GND electrode of a large area is disposed between the upper and lower chips 2, 7, it is possible to improve the effect of electromagnetic shielding between both chips and hence possible to prevent

interference between the first-/second-stage amplifiers and the last-stage (third-stage) amplifier.

That is, it is possible to strengthen the electromagnetic shielding between the control circuit, as well as the first- and second-stage amplifier circuits, and the third-stage amplifier circuit and hence possible to prevent the occurrence of inconveniences such as oscillation in a frequency band other than the predetermined frequency band.

Consequently, it is possible to improve the reliability of the power amplifier module 1.

Further, since GND of the upper chip 2 is strengthened and stabilized by the common electrode 12, even if the second-stage amplifier circuit is incorporated in the upper chip 2, GND of the upper chip 2 does not become unstable and it is possible to improve the reliability of the power amplifier module 1.

Plural chip parts 3 as passive parts mounted around the semiconductor chip on the main surface 4b of the module substrate 4 are, for example, chip resistors and chip capacitors, and connecting terminals 3a formed at both ends of the chip components are connected, for example, by soldering to the terminals 4e formed on the module substrate 4.

A description will now be described of a power amplifier 1 according to a modification of the first embodiment. In the power amplifier module 1 shown in Fig. 6, an IPD (Integrated Passive Device) chip 15 formed by plural chip parts 3 as

components is mounted on a module substrate 4. More specifically, a single IPD chip 15 incorporating plural such elements as resistor, capacitor and inductance elements is mounted on the module substrate 4, whereby the number of chip parts 3 mounted on the module
substrate 4 is decreased, thereby permitting a further reduction in size of the power amplifier module 1.

Since such elements as resistor, capacitor and inductance elements are incorporated in the IPD chip 15, there is adopted a glass substrate, for example and the elements are formed on the glass substrate.

In a power amplifier module 1 according to another modification of the first embodiment, there is used a module substrate 4 not having such a cavity 4a as shown in Fig. 1 that is a recess but having a flat main surface 4b.
A lower chip 7 is flip-connected to the flat main surface 4b of the module substrate 4 and an upper chip 2 is stacked face up onto the lower chip 7. Thus, the power amplifier module 1 of Fig. 7 is of such a stacked chip structure.

In the power amplifier module 1 shown in Fig. 7, the shape of the module substrate 4 illustrated therein can be obtained easily, so that it is possible to reduce the cost of the module substrate 4 and hence reduce the cost of the power amplifier module 1.

(Second Embodiment)

Fig. 8 is a sectional view showing the structure of a power amplifier module as an example of a semiconductor device according to a second embodiment of the present invention, Fig. 9 is a back view thereof, and Fig. 10 is a planar layout diagram showing a layout example of parts mounted on a main surface of a wiring substrate in the power amplifier module.

As is the case with the first embodiment, the semiconductor device of this second embodiment shown in Fig. 8 is a power amplifier module 16. The power amplifier module 16 is different from the power amplifier module 1 of the first embodiment in that a lower chip (second semiconductor chip) 7 is mounted face up on a module substrate 4 and an upper chip (first semiconductor chip) 2 is stacked face up on the lower chip and that a spacer 17 is disposed between the lower chip 7 and the upper chip 2.

More specifically, the lower chip 7 is mounted face up on the module substrate 4 by soldering and the upper chip 2 is stacked face up on the upper chip 2 through the spacer 17. Further, since both lower and upper chips 7, 2 are mounted face up, both are connected to the module substrate 4 through electrically conductive wires 5 such as gold wires.

As is the case with the power amplifier module 1 of the first embodiment, a common electrode 12 as an electrode of a fixed potential is formed on a back surface 2b of the upper chip 2 and a common electrode 12 is formed also on a main

surface 17a of the spacer 17 whose main surface is opposed to the upper chip 2, both common electrodes 12 being connected together using Ag paste 8 (see Fig. 5) as in the first embodiment.

Therefore, a semiconductor substrate 13 (see Fig. 5) of the upper chip 2 is electrically connected to the common electrodes 12.

The common electrodes 12 used in this second embodiment are the same as the common electrodes 12 used in the first embodiment illustrated in Fig. 5 and are used as GND electrodes of a large area. Further, wires 5 are connected to the common electrode 12 formed on a projecting portion 17b of the spacer 17 projecting from the upper chip 2 and, as shown in Fig. 10, the wires 5 are connected to terminals 4d for GND formed on the module substrate 4.

Thus, as GND electrode on the upper chip 2 side there may be adopted the common electrode 12 of a large area formed on the back surface 2b of the upper chip, and the common electrode 12 and the module substrate 4 are electrically connected with each other through plural wires 5 connected to the common electrode 12.

With the above arrangement, GND of the upper chip 2 can be strengthened as is the case with the power amplifier module 1 of the first embodiment.

Further, as in the first embodiment, the common electrode

12 as GND electrode of a large area can be disposed between the upper chip 2 and the lower chip 7.

In the power amplifier module 16 of this second embodiment, the lower chip 7 is mounted face up on the module substrate 4, therefore, as shown in Fig. 8, GND of the lower chip 7 is connected to plural via holes 4h formed in the module substrate 4 through a semiconductor substrate (see Fig. 5) of the lower chip and further through a back surface 7b of the lower chip and is further connected to an external terminal 4g for GND formed on a back surface 4c, whereby GND of the lower chip is strengthened.

Although the spacer 17 disposed between the lower chip 7 and the upper chip 2 is formed of silicon for example, it may be formed of any other insulating material than silicon. The spacer 17 is for spacing between the lower chip 7 and the upper chip 2, and by disposing the spacer 17 between both chips it is possible to prevent contact between the wires 5 connected to the lower chip 7 and the wires 5 connected tot he spacer 17 and also prevent contact of the wires 5 connected to the lower chip 7 with the upper chip 2.

Further, since the connection between the spacer 17 and the lower chip 7 is effected using an insulating adhesive, GND of the upper chip 2 and GND of the lower chip 7 are not used in common.

The circuit configuration of the power amplifier module 16

of this second embodiment is the same as that of the power amplifier module 1 of the first embodiment illustrated in Fig. 4. That is, correspondingly to circuit blocks 2e and 7e, GSM-side first- and second-stage amplifiers 2c, 2f and DCS-side first- and second-stage amplifiers 2d, 2g are incorporated in the upper chip 2, while a GSM-side last-stage (third-stage) amplifier 7c and a DCS-side last-stage (third-stage) amplifier 7d are incorporated in the lower chip 7.

A control IC 2h is also incorporated in the upper chip 2.

As shown in Fig. 9, as is the case with the power amplifier module 1 of the first embodiment, plural external terminals 4f and an external terminal 4g for GND are formed on the back surface 4c of the module substrate 4 in the power amplifier module 16.

According to the power amplifier module 16 of this second embodiment, there can be obtained the same effects as in the power amplifier module 1 of the first embodiment; besides, since the lower chip 7 is mounted face up on the module substrate 4, GND of the lower chip 7 can be connected from its back surface 7b side to the external terminal 4g for GND on the back surface 4c through plural via holes 4h formed in the module substrate 4, whereby GND of the lower chip 7 can be further strengthened.

Although the present invention has been described above concretely on the basis of embodiments thereof, it goes without

saying that the present invention is not limited to the above embodiments and that various changes may be made within the scope not departing from the gist of the invention.

For example, although in the above first and second embodiments reference has been made to the case where the semiconductor device is a power amplifier module, the semiconductor device may be any other module product than the power amplifier module insofar as the module product is of a structure in which plural semiconductor chips are stacked on the main surface 4b of the module substrate 4. In this case, the number of semiconductor chips to be stacked is not limited to two stages, but may be three or more stages.

Effects obtained by typical modes of the present invention as disclosed herein will be outlined below.

In a stacked chip type semiconductor device, a lower chip is mounted by flip connection, whereby it is possible to eliminate a difference in size between upper and lower chips and hence possible to reduce the area of the semiconductor device and attain the reduction in size of the semiconductor device.